

# Tmap

Dual 3D

**FOGALE nanotech**

## Metrology solution for 3D IC/TSV process control

### *Unique on the market*

Patented optical head combining IR and white light microscopy with metrology in the same optical path.



### *Applications:*

- TSV formation ✓
- Temporary carrier process ✓
- Thinning process ✓
- Stacking process ✓

### *Benefits:*

- Metrology and vision in the same optical path ✓
- Combination of IR & WL microscopy ✓
- Multiple sensor configurations ✓
- Address all 3D IC/TSV main process steps ✓

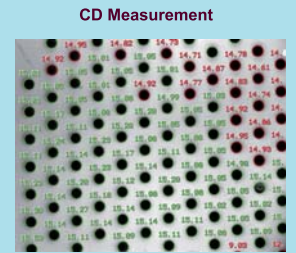
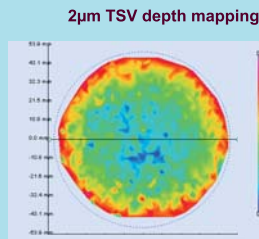
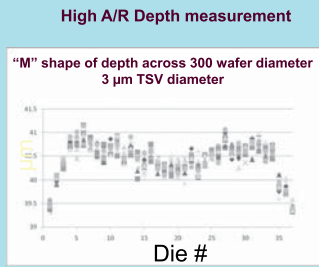
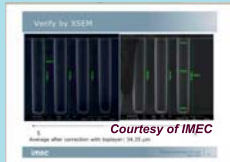
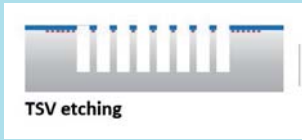
# T-MAP DUAL 3D 300A

## FULL Process control solution for 3D IC TSV

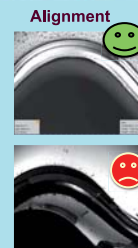
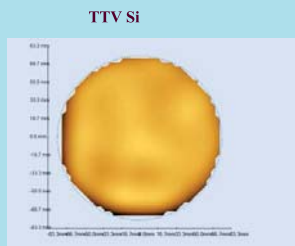
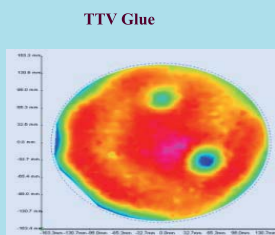
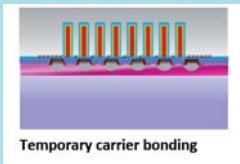


### From TSV etching to TSV Reveal and die stacking: Inspection and metrology

#### ✓ TSV Etching: CD and Depth



#### ✓ Temporary Bonding: Thickness, TTV, Glue Thickness uniformity, RST and defect/Void detection ...



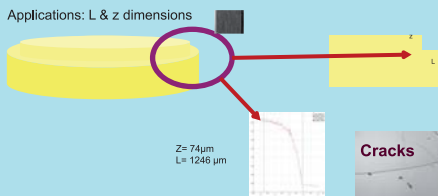
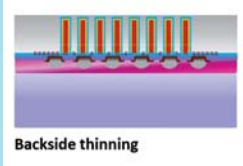
Interface micro inspection  
➢ down to 1 μm resolution



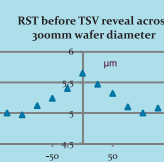
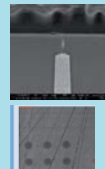
Interface macro inspection (full wafer)  
➢ down to 25 μm resolution



#### ✓ Backside thinning: Edge trim, RST and roughness measurement, Cracks defect review

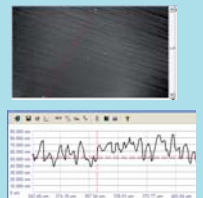


Edge inspection

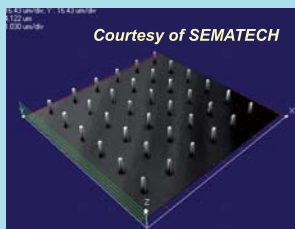
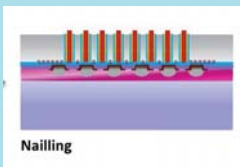


Influence of TSV depth uniformity + Wafer thinning

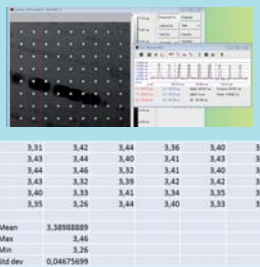
Backside Roughness



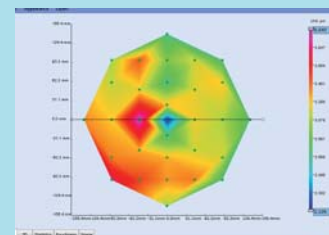
#### ✓ TSV reveal: Height and Co-planarity



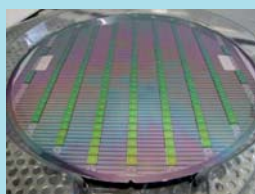
Height and co-planarity



Pillar height uniformity within wafer



#### ✓ Stacking



SMARTSTACK Project: FOGALE, LETI, ST GEMALTO, SPTS

