

EVG® GEMINI®FB XT

Fully-Automated Fusion Bonding System for Future 3D Devices

Introduction

While wafer-to-wafer fusion bonding has predominantly been used for high-volume manufacturing of backside illuminated (BSI) image sensors, front-end-of-line 3D device stacking as well as novel BSI image sensors demand improved overlay alignment. EVG's GEMINI FB XT integrated fusion bonding system extends current standards and combines higher productivity with improved face-to-face alignment accuracy. The system features the completely new developed SmartView NT2 bond aligner, which breaks future alignment requirements of 200nm (3σ).

3x improvement in wafer-to-wafer alignment

- New SmartView®NT2
- Better than 200nm (3σ) face-to-face alignment

50% increased throughput

- Upgrade to six pre-processing modules
- Faster handling and improved process flows

Enabling new devices

- 3D stacked memory (high bandwidth memory, etc.)
- Next-generation stacked CMOS image sensors
- Monolithic device architecture



GEMINI®FB XT

Technical Data

Maximum wafer size	200 mm / 300 mm
Minimum processable wafer size	100 mm / 150 mm
Alignment Accuracy	< 200nm (3σ)
Maximum Number of Preprocessing Modules	6
Preprocessing Modules	<ul style="list-style-type: none"> - Clean Module - LowTemp™ Plasma Activation Module - Alignment Verification Module - Debond Module - Inline Metrology Module
Typical customer application	Fusion Bonding for Backside Illuminated Image Sensors, Memory Stacking and Stacking of Future 3D Devices

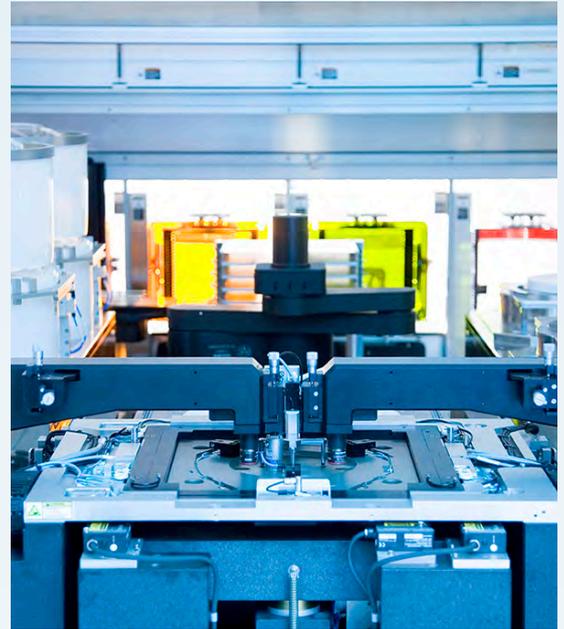


Fusion Bonding for Future 3D Devices

While wafer-to-wafer fusion bonding has predominantly been used for high-volume manufacturing of backside illuminated (BSI) image sensors, front-end-of-line 3D device stacking as well as novel BSI image sensors demand improved overlay alignment. EVG's GEMINI FB XT integrated fusion bonding system extends current standards and combines higher productivity with improved face-to-face alignment accuracy. The system features the completely new developed SmartView NT2 bond aligner, which breaks future alignment requirements of 200nm (3σ). Minimizing through silicon via (TSV) dimensions for via-last bonding, or TSV and bonding pad dimensions for hybrid bonding, are key requirements for bringing down the cost of 3D devices. Considering that the role of a TSV is essentially "only" for signal connection yet consumes valuable wafer real estate, further miniaturization has to be the logical consequence.

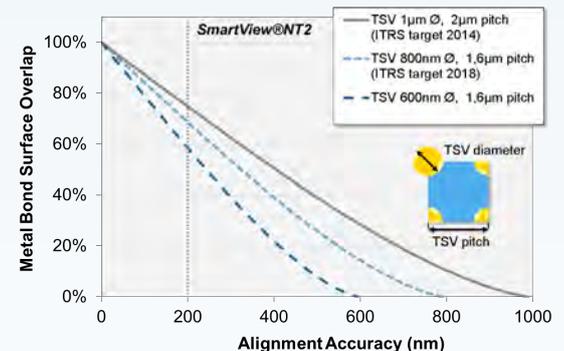
A first option for high-bandwidth integration is hybrid bonding, whereby a dual damascene copper and silicon oxide hybrid interface serves as both the full-area bonding mechanism and the electrical connection. A second option is the transfer of a thin processed semiconductor layer (ranging from tens to a few hundred nanometers in thickness) using a full-area dielectric bond. In contrast to hybrid bonding, the electrical connection is introduced by a via-last process between early interconnect metal levels on the bottom wafer and the second transferred transistor layer. Both hybrid bonding and full-area dielectric bonding can be achieved through aligned wafer-to-wafer fusion bonding. However, high-interconnect density along with small routing dimensions set a high bar for bond alignment precision, which is necessary for fusion bonding.

Several factors contribute to the global alignment of the wafers besides the in-plane measurement and placement of the wafers relative to each other. In fusion bonding, both wafers are aligned and a pre-bond is initiated. When bringing the device wafers together, wafer stress and/or bow can influence the formation of a bond wave. The bond wave describes the front where hydrogen bridge bonds are formed to pre-bond the wafers. Controlling the continuous wave formation and influencing parameters is key to achieving the tight alignment specifications noted above. The reason for this is that any wafer strain manifests in distortion of the wafer, which leads to an additional alignment shift. Process and tool optimization can minimize strain and significantly reduce local stress patterns. Typically, distortion values in production are well below 50nm. Indeed, further optimization of distortion values is a combination of many factors, including not only the bonding process and equipment, but also previous manufacturing steps and the pattern design.



	Epitaxial Growth	Hybrid Bonding	Via-last Integration
	600-1000°C epi growth	pad-to-pad via-to-via via-to-pad	via-last
Integration Density	Medium	High	Medium
Process Temperature	600-1000°C	200-400°C	200-300°C
Process Readiness	Not ready	Yes	Yes
Die Yield	Low	High	High
Complexity	High	Medium	Medium

Comparison of different 3D front-end-of-line integration schemes.



Calculated surface overlap of metal TSVs for hybrid bonding as a function of wafer-to-wafer alignment accuracy. Comparison of ITRS roadmap relevant TSV pitches and diameters reveal, alignment accuracy of better than 200nm (3σ) is needed to achieve 60% and more TSV overlap for hybrid bonding.

