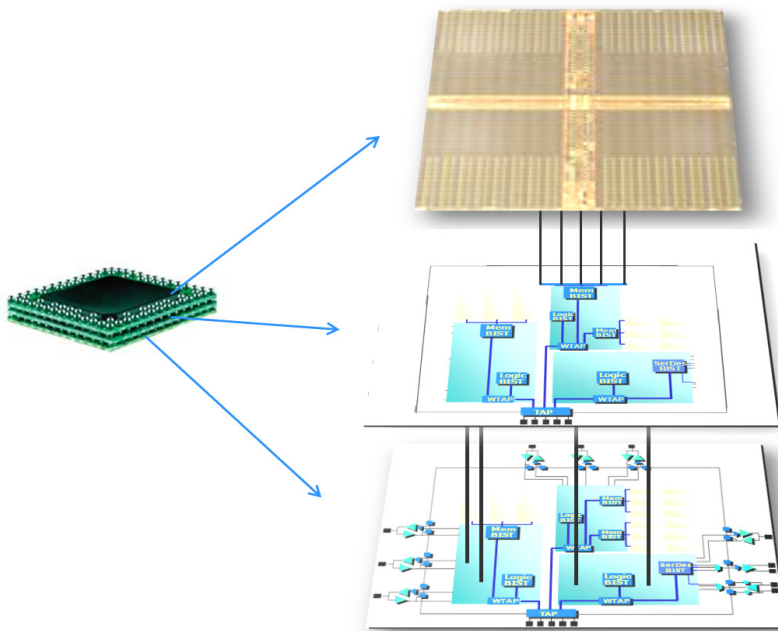


# Tessent

## Support for Testing 3D-ICs

### Silicon Test and Yield Analysis

### D A T A S H E E T



### Key Benefits

- Test 3D-ICs today with available Tessent<sup>®</sup> technology.
- Improve yield of stacked die with high-quality test of single die components.
- Generate test patterns for stacked die faster by retargeting existing single die patterns using the same test generation methods.
- Mentor Graphics award-winning customer support ensures success.

### Challenges in Testing 3D-IC Designs

Three-dimensional stacked integrated circuits (3D-ICs) are composed of multiple stacked die, and are viewed as critical in helping the semiconductor industry keep pace with Moore's Law. Current integration and interconnect methods include wirebond and flip-chip and have been in production for some time.

The next generation of 3D integration incorporates through-silicon-via (TSV) technology as the primary method of interconnect between the die. The migration to 3D-ICs connected by TSVs presents three new test challenges to the industry:

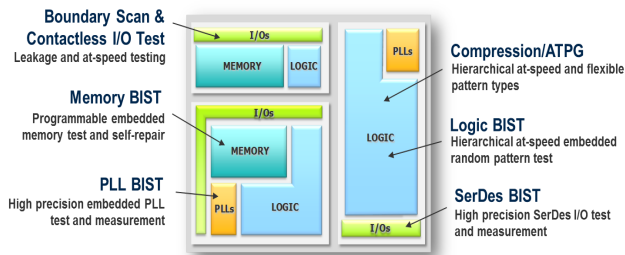
1. Managing the escape rate of defective die at wafer to meet target post-packaging yield.
2. Testing memory die stacked on logic die configurations.
3. Testing logic stacked on logic die configurations.

### Comprehensive Solutions for Known Good Die

The Tessent<sup>®</sup> silicon test and yield analysis solutions provide a comprehensive set of design-for-test (DFT) capabilities that addresses the known-good-die testing challenges. These include the industry-leading solutions for ATPG, compression, logic BIST, memory BIST, boundary scan, mixed-signal BIST and silicon learning.

### Key Features

- Tessent 3D-IC support is included in the TSMC Reference Flow 12.
- Comprehensive test generation, DFT and BIST capabilities enable low-cost, high-quality test for meeting critical known-good-die (KGD) requirements.
- Programmable external memory BIST enables thorough at-speed testing of memory-to-logic TSVs.
- Hierarchical ATPG enables efficient testing of logic to logic TSVs.



The Tessent product family for silicon test and yield analysis provide solutions for 2.5D and 3D ICs

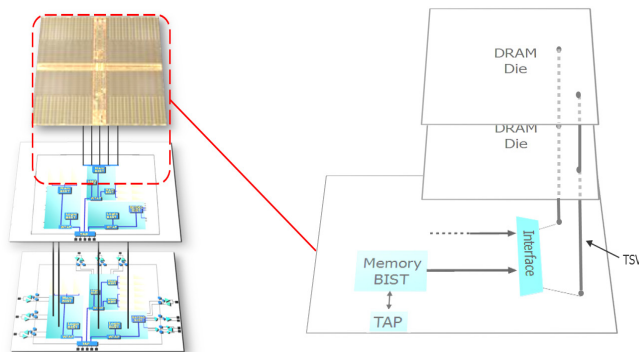
## Testing Stacked Memory-on-Logic

Using Tessent's integrated hierarchical test capabilities, high-quality tests can be implemented for stacked logic and memory die.

Tessent MemoryBIST provides at-speed testing of stacked memory die with support for all popular DRAM protocols, and allows memory parameters (address size, waveforms) and test algorithms to be programmed post-silicon. This allows memory BIST controllers in a logic die to handle a variety of memory die stacked on top for different product variations. Tessent also supports at-speed testing of memory buses, which covers both bond wires and TSV interconnects. A shared-bus capability enables test of multiple memory die on the same interconnect.

## Testing Stacked Logic-on-Logic

For logic-on-logic stacks, the Tessent hierarchical test capabilities are used to test the stacked die and the TSV interconnects.



Using Tessent solutions to test memory stacked on logic.

The ATPG and BIST tests that were generated for single die testing are reused, saving test development times. The patterns are resequenced as required to ensure correct pattern distribution and application across multiple die.

The Tessent hierarchical ATPG solution is used to test TSVs between logic die. These TSVs are assumed to exist between the boundaries of scan isolated cores on neighboring die. Test patterns are generated using the full package netlist where a graybox model is used for non-targeted die and/or cores.

By using a combination of hierarchical test architecture, high compression scan testing, and BIST technologies, the Mentor Graphics Tessent solution provides the highest quality and most economical 3D-IC testing available.

## Tessent Silicon Test and Yield Analysis Solutions

All Tessent tools are available on UNIX and Linux. For more information, visit [www.mentor.com](http://www.mentor.com).

### The Tessent Product Line

#### Logic Test

Tessent<sup>®</sup> TestKompress<sup>®</sup>  
Tessent LogicBIST  
Tessent SoCScan  
Tessent FastScan<sup>™</sup>  
Tessent BoundaryScan

#### Mixed-Signal Test

Tessent SerdesTest  
Tessent PLLTest

#### Silicon Learning

Tessent SiliconInsight<sup>®</sup>  
Tessent YieldInsight<sup>®</sup>  
Tessent Diagnosis

#### Memory Test

Tessent MemoryBIST

For more information about 3D-IC test support, download the white paper *Testing 3D-ICs with Tessent* from [http://go.mentor.com/3D-IC\\_Test](http://go.mentor.com/3D-IC_Test)

## Visit our website at [www.mentor.com](http://www.mentor.com)

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